IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of: **Masaharu YAMAMOTO et al.** Art Unit: **2818**

Application Number: **10/568,075** Examiner: **Jonathan Han**

Filed: **February 13, 2006** Confirmation Number: **7448**

For: **HERMETIC SEALING CAP, METHOD OF MANUFACTURING HERMETIC SEALING CAP AND ELECTRONIC COMPONENT STORAGE PACKAGE**

Attorney Docket Number: **062092**
Customer Number: **38834**

SUBMISSION OF APPEAL BRIEF

Mail Stop: Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

September 20, 2010

Sir:

Applicants submit herewith an Appeal Brief in the above-identified U.S. patent application.

Attached please find a check in the amount of $540.00 to cover the cost for the Appeal Brief. If any additional fees are due in connection with this submission, please charge Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP

/SADAO KINASHI/

Sadao Kinashi
Attorney for Appellants
Registration No. 48,075
Telephone: (202) 822-1100
Facsimile: (202) 822-1111

SK/kn

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPEAL BRIEF FOR THE APPELLANTS

Ex parte Masaharu YAMAMOTO et al. (Appellants)

HERMETIC SEALING CAP, METHOD OF MANUFACTURING HERMETIC SEALING CAP AND ELECTRONIC COMPONENT STORAGE PACKAGE

Application Number: **10/568,075**

Filed: **February 13, 2006**

Appeal No.: **Not Yet Assigned**

Art Unit: **2818**

Examiner: **Jonathan Han**

Submitted by:
Sadao Kinashi
Registration No. 48,075
Attorney for Appellants

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 Connecticut Avenue NW, Suite 700
Washington, D.C. 20036
Tel (202) 822-1100
Fax (202) 822-1111

September 20, 2010

BRIEF ON APPEAL

(I) REAL PARTY IN INTEREST

The real party in interest is **NEOMAX MATERIALS CO., LTD.**, by an assignment recorded in the U. S. Patent and Trademark Office on **February 13, 2006**, at Reel **017579**, Frame **0994**.

(II) RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to appellant, appellant's legal representative, or assignee that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(III) STATUS OF CLAIMS

Claims 1-20 are pending in the application. Claims 1-20 are rejected and all the rejected claims are appealed. The appealed claims appear in the Claims Appendix.

(IV) STATUS OF AMENDMENTS

No amendments have been filed subsequent to the close of prosecution.

(V) SUMMARY OF THE INVENTION

An electronic component storage package such as an SMD (Surface Mount Device) package (surface mount device package) employed for hermetically sealing an electronic component such as a SAW filter (surface acoustic wave filter) or a crystal oscillator employed for noise removal of a portable telephone or the like is known in general. Such an electronic component storage is constituted of an electronic component storing member on which the electronic component is mounted and a hermetic sealing cap hermetically sealing the electronic component storing member. This hermetic sealing cap is heated to be bonded to the electronic component storing member through a solder layer. Thereafter the electronic component package is reheated to be mounted on a printed wiring board of an electronic apparatus or the like. (Page 1, line 15 to page 2, line 3, also see Fig. 8).

WO02/078085 discloses an electronic component package employing a lid body (hermetic sealing cap) integrally formed by arranging an Ni group metal layer on the upper surface of a core portion (substrate) while superposing an Ni alloy layer diffusing into a brazing filler metal layer in hermetic sealing and the brazing filler metal layer (solder layer) on the lower surface in this order and thereafter pressure-welding/bonding these four layer members to each other. (Page 2, line 24 to page 3, line 8).

When the solder layer is formed by arranging the solder paste on the sealed portion of the lower surface of the Ni alloy layer and thereafter melting the solder paste in the structure of WO02/078085, however, there is a problem that an intermetallic compound is formed in the

solder layer and the melting point of the solder layer increases when forming the solder layer by melting the solder paste. Such a solder layer is hard to melt when bonding the hermetic sealing cap to an electronic component storing member by melting the solder layer after formation of the solder layer. Consequently, there is such a problem that wettability of the solder layer with respect to the electronic component storing member so lowers that air-tightness of the electronic component storing package may lower. (Page 4, line 15 to page 5, line 7).

When the drawings are referred to for the purpose of understanding, the hermetic sealing cap (1) according to claim 1 has a substrate (2), and a first layer (3) is formed on the surface of the substrate. The first layer (3) is mainly composed of Ni containing a diffusion accelerator. The hermetic sealing cap (1) also has a second layer (4) formed in contact with the surface of the first layer and a solder layer (5) mainly composed of Sn formed on a region of the surface of the second layer (4) to which the electronic component storing member is bonded. The second layer (4) is formed so as to inhibit the first layer (3) from diffusing into the solder layer (5) at a first temperature. However, the first layer (3) diffuses into the solder layer (5) through the second layer (4) when the solder layer (5) bonds to the electronic component storing member at a second temperature higher than the first temperature.

(VI) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-3, 5-10, 12-14, and 16-20 are rejected under 35 U.S.C. 103(a) for allegedly being obvious over Levine (U.S. Patent No. 4,666,796) in view of Kim et al. (U.S. Publication No. 2003/0104651 A1) and Suzuki (Japanese Publication No. 2005-123297A).

Claims 4 and 15 are rejected under 35 U.S.C. 103(a) for allegedly being obvious over Levine (U.S. Patent No. 4,666,796) in view of Kim et al. (U.S. Publication No. 2003/0104651 A1) and Suzuki (Japanese Publication No. 2005-123297 and further in view of Woolhouse et al. (U.S. Patent No. 4,236,296; hereinafter referred to as Woolhouse).

Claim 11 is rejected under 35 U.S.C. 103(a) for allegedly being over Levine (U.S. Patent No. 4,666,796) in view of Kim et al. (U.S. Publication No. 2003/0104651 A1) and Suzuki (Japanese Publication No. 2005-123297 A), and further in view of Shiomi et al. (U.S. Publication No. 2004/0023487 A1; hereinafter referred to as Shiomi).

(VII) ARGUMENT

1. Claims 1-3, 5-10, 12-14, and 16-20 are Not Obvious Under 35 U.S.C. 103(a) Over Levine In View Of Kim et al. And Suzuki.

Claims 1-3, 5-10, 12-14, and 16-20 stand rejected for allegedly being obvious under 35 U.S.C. 103(a) over Levine (U.S. Patent No. 4,666,796) in view of Kim et al. (U.S. Publication No. 2003/0104651 A1) and Suzuki (Japanese Publication No. 2005-123297A).

Admitting that Levine fails to disclose "a first layer . . . containing a diffusion accelerator," "a solder layer mainly composed of Sn formed on a region of the surface of said second layer to which said electronic component storing member is bonded, wherein said second layer is formed so as to inhibit said first layer from diffusing into said solder layer at a first temperature and diffuse said first layer into said solder layer through said second layer when said solder layer bonds to said electronic component storing member at a second temperature higher

than said first temperature," the Examiner cited Suzuki, and alleged that Suzuki discloses a first layer contains a diffusion accelerator referring to paragraph [0033]-[0034], and noted that cobalt is a diffusion accelerator. (Office Action of 12/04/2009, page 3). Suzuki describes as follows:

> [0034]
> In the wiring board of this invention, the **nickel-cobalt layer 10 is formed directly under the gold layer 11**. Since **a cobalt component inhibits diffusion of nickel components**, part of nickel in the nickel layer 9 or the nickel-cobalt layer 10 is neither diffused into the inside of the gold layer 11, nor exposed to be oxidized on the surface of the gold layer 11. Thus, a nickel oxide or a nickel hydroxide having bad wettability with respect to the solder material 8 is hardly generated, whereby bonding the metallized layer 6 for sealing and the solder material 8 becomes strengthened, and bonding the metallized layer 6 for sealing and the metal lid body 2 through the solder material 8 reliably becomes further strengthened.

(Suzuki, paragraph [0034]). Because of the difference in the function of the layers the order of the layers is also different. According to Suzuki, when assuming that the gold layer is the solder layer, the order of the layers is Ni/ Ni-Co/Au. In contrast, according to claim 1, where the diffusion accelerator is Co, the order of the layers is Ni-Co/Ni/solder layer. Thus, the order of the layers is different between Suzuki and the present invention. Therefore, even the teaching of Suzuki is combined with Levine, there is no reason that the hermetic sealing cap structure recited in claim 1 is obtained.

Then the Examiner alleged:

> Suzuki fails to disclose a solder layer mainly composed of Sn formed on a region of the surface of said second layer to which said electronic component storing member is bonded, wherein said second layer is formed so as to inhibit said first layer from diffusing into said solder layer at a first temperature and diffuse said first layer into said solder layer through said second layer when said solder layer bonds to said

> electronic component storing member at a second temperature higher than said first temperature.

(Office Action of 12/04/2009, page 3). However, Kim et al. simply describes Sn as an example of the materials to form a solder layer of a particular lid frame.

Therefore, even if Levine is combined with Suzuki and Kim et al., there is no reason to make a sealing cap comprising "a substrate; a first layer, formed on the surface of said substrate, mainly composed of Ni containing a diffusion accelerator; a second layer formed **to be in contact with** the surface of said first layer; and a solder layer mainly composed of Sn formed on a region of the surface of said second layer to which said electronic component storing member is bonded, wherein said second layer **is formed so as to inhibit** said first layer from diffusing into said solder layer at a first temperature **and diffuse** said first layer into said solder layer through said second layer when said solder layer bonds to said electronic component storing member at a second temperature higher than said first temperature."

The Examiner alleged in the Advisory Action as follows:

> Applicant argued that Suzuki does not disclose the utilization of a diffusion accelerator as cobalt inhibits diffusion of nickel components based on applicant's translation. However, accelerators are not limited to speeding up a reaction. An accelerator changes the speed of the reaction, whether slower or faster. Acceleration is a change in the speed, not an increase, therefore, cobalt's control of the diffusion rate constitutes a diffusion accelerator.

(Advisory Action, continuation sheet). However, the Examiner's allegation ignores ordinary meaning and the consistent use of the word "accelerator" in the present specification.

According to the present invention, the first layer can be easily diffused into the solder layer through the second layer when the solder layer bonds to the electronic component storing member at the second temperature higher than the first temperature as compared with a case where the second layer is not directly in contact with the surface of the first layer. This is not expected from Levine and Suzuki.

For at least these reasons, claim 1 patentably distinguishes over Levine, Suzuki and Kim et al.

For the substantially same reasons, independent claims 10 also patentably distinguish over Levine, Suzuki and Kim et al.

Similarly, regarding claim 12, none of Levin, Kim et al. and Suzuki discloses or suggests, among other things, "preparing a substrate; forming a first layer mainly composed of Ni containing a diffusion accelerator on the surface of said substrate; forming a second layer on the surface of said first layer; and forming a solder layer mainly composed of Sn at a first temperature on a region of the surface of said second layer to which said electronic component storing member is bonded with the second layer inhibiting said first layer from diffusing into said solder layer at the first temperature," For at least these reasons, claim 12 patentably distinguishes over Levine, Suzuki and Kim et al.

Because independent claims 1, 10 and 12 are patentably distinguish over the prior art, dependent claims also patentably distinguish over the prior art for at least the same reasons.

2. Claims 4 and 15 are Not Obvious under 35 U.S.C. 103(a) Over Levine in view of Kim et al. and Suzuki and further in view of Woolhouse et al.

Claims 4 and 15 stands rejected under 35 U.S.C. 103(a) for allegedly being obvious over Levine (U.S. Patent No. 4,666,796) in view of Kim et al. (U.S. Publication No. 2003/0104651 A1) and Suzuki (Japanese Publication No. 2005-123297 and further in view of Woolhouse et al. (U.S. Patent No. 4,236,296).

Claim 4, depending from claim 1, and claim 15, indirectly depending from claim 12, patentably distinguish over Levine, Suzuki and Kim et al. for at least the same reasons as discussed above.

Woolhouse et al. has been cited for allegedly disclosing second layer has a thickness of at least 0.03 pm and not more than 0.075 pm. However, such a disclosure of Woolhouse et al. does not remedy the deficiencies of Levine, Suzuki and Kim et al.

For the substantially same reasons, claims 4 and 15 patentably distinguish over Levine, Suzuki, Kim et al. and Woolhouse et al.

3. Claim 11 is Not Obvious under 35 U.S.C. 103(a) Over Levine in view of Kim et al. and Suzuki, and further in view of Shiomi et al.

Claim 11 stands rejected under 35 U.S.C. 103(a) for allegedly being obvious over Levine (U.S. Patent No. 4,666,796) in view of Kim et al. (U.S. Publication No. 2003/0104651 A1) and Suzuki (Japanese Publication No. 2005-123297 A), and further in view of Shiomi et al. (U.S. Publication No. 2004/0023487 A1).

Claim 11, depending from claim 10, patentably distinguishes over Levine, Suzuki and Kim et al. for at least the same reasons as discussed above.

Shiomi et al. has been cited for allegedly disclosing the junction between said hermetic sealing cap and said electronic component storing member contains an intermetallic compound consisting of an Ni-Sn alloy. However, such disclosures of Shiomi et al. do not remedy the deficiencies of Levine, Suzuki and Kim et al.

For the substantially same reasons, claim 11 patentably distinguishes over Levine, Suzuki, Kim et al. and Shiomi et al.

(VIII) CONCLUSION

For the foregoing reasons, the Examiner has failed to establish a prima facie case of obviousness in the rejection of the present claims. The Honorable Board is respectfully requested to reverse the rejection of the Examiner.

If this paper is not timely filed, appellants hereby petition for an appropriate extension of time. The fee for any such extension may be charged to Deposit Account No. 50-2866, along with any other additional fees that may be required with respect to this paper.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP

/SADAO KINASHI/

Sadao Kinashi
Attorney for Applicants
Registration No. 48,075
Telephone: (202) 822-1100
Facsimile: (202) 822-1111

SK/kn
Enclosures: Claims Appendix
Evidence Appendix
Related Proceedings Appendix

(IX) CLAIMS APPENDIX

1. (Rejected): A hermetic sealing cap employed for an electronic component storage package including an electronic component storing member for storing an electronic component, comprising:

a substrate;

a first layer, formed on the surface of said substrate, mainly composed of Ni containing a diffusion accelerator;

a second layer formed to be in contact with the surface of said first layer; and

a solder layer mainly composed of Sn formed on a region of the surface of said second layer to which said electronic component storing member is bonded,

wherein said second layer is formed so as to inhibit said first layer from diffusing into said solder layer at a first temperature and diffuse said first layer into said solder layer through said second layer when said solder layer bonds to said electronic component storing member at a second temperature higher than said first temperature.

2. (Rejected): The hermetic sealing cap according to claim 1, wherein

said first temperature is a temperature at a time of forming said solder layer by melting solder paste, and

said second temperature is a temperature at a time of bonding said hermetic sealing cap to said electronic component storing member by melting said solder layer.

3. (Rejected): The hermetic sealing cap according to claim 1, wherein said second layer is made of Ni.

4. (Rejected): The hermetic sealing cap according to claim 3, wherein said second layer has a thickness of at least 0.03 μm and not more than 0.075 μm.

5. (Rejected): The hermetic sealing cap according to claim 1, wherein said first layer contains 7.5 mass % to 20 mass % of Co as said diffusion accelerator.

6. (Rejected): The hermetic sealing cap according to claim 1, wherein said substrate is made of an Fe-Ni-Co alloy.

7. (Rejected): The hermetic sealing cap according to claim 1, wherein said first layer and said second layer are formed by plating.

8. (Rejected): The hermetic sealing cap according to claim 7, wherein said first layer is formed on the whole area of the surface of said substrate, and said second layer is formed on the whole area of the surface of said first layer.

9. (Rejected): The hermetic sealing cap according to claim 1, wherein said solder layer contains no Pb, and contains Ag.

10. (Rejected): An electronic component storage package including an electronic component storing member for storing an electronic component, comprising:

a hermetic sealing cap including

a substrate,

a first layer, formed on the surface of said substrate, mainly composed of Ni containing a diffusion accelerator,

a second layer formed to be in contact with the surface of said first layer, and

a solder layer mainly composed of Sn formed on a region of the surface of said second layer to which said electronic component storing member is bonded,

wherein said second layer is formed so as to inhibit said first layer from diffusing into said solder layer at a first temperature and diffuse said first layer into said solder layer through said second layer when said solder layer bonds to said electronic component storing member at a second temperature higher than said first temperature,

wherein a third layer is formed on a portion of said electronic component storing member corresponding to said solder layer,

said solder layer and said third layer are bonded to each other, and

an intermetallic compound containing Sn of said solder layer is formed on the junction between said hermetic sealing cap and said electronic component storing member.

11. (Rejected): The electronic component storage package according to claim 10, wherein

the junction between said hermetic sealing cap and said electronic component storing member contains an intermetallic compound consisting of an Ni-Sn alloy, and

a portion of said second layer corresponding to the junction between said hermetic sealing cap and said electronic component storing member diffuses in said intermetallic compound.

12. (Rejected): A method of manufacturing a hermetic sealing cap employed for an electronic component storage package including an electronic component storing member for storing an electronic component, comprising steps of:

preparing a substrate;

forming a first layer mainly composed of Ni containing a diffusion accelerator on the surface of said substrate;

forming a second layer on the surface of said first layer; and

forming a solder layer mainly composed of Sn at a first temperature on a region of the surface of said second layer to which said electronic component storing member is bonded with the second layer inhibiting said first layer from diffusing into said solder layer at the first temperature,

wherein said second layer is formed such that said first layer diffuses into said solder layer through said second layer when said solder layer bonds to said electronic component storing member at a second temperature higher than said first temperature.

13. (Rejected): The method of manufacturing a hermetic sealing cap according to claim 12, wherein

the step of forming said solder layer includes steps of arranging solder paste mainly composed of Sn on a region of the surface of said second layer to which said electronic component storing member is bonded and forming said solder layer mainly composed of said Sn by melting said solder paste at said first temperature.

14. (Rejected): The method of manufacturing a hermetic sealing cap according to claim 12, wherein

said second layer is made of Ni.

15. (Rejected): The method of manufacturing a hermetic sealing cap according to claim 14, wherein

said second layer has a thickness of at least 0.03 μm and not more than 0.075 μm.

16. (Rejected): The method of manufacturing a hermetic sealing cap according to claim 12, wherein

said first layer contains 7.5 mass % to 20 mass % of Co as said diffusion accelerator.

17. (Rejected): The method of manufacturing a hermetic sealing cap according to claim 12, wherein

said substrate is made of an Fe-Ni-Co alloy.

18. (Rejected): The method of manufacturing a hermetic sealing cap according to claim 12, wherein

the step of forming said first layer includes a step of forming said first layer by plating, and

the step of forming said second layer includes a step of forming said second layer by plating.

19. (Rejected): The method of manufacturing a hermetic sealing cap according to claim 18, wherein

the step of forming said first layer by plating includes a step of forming said first layer on the whole area of the surface of said substrate, and

the step of forming said second layer by plating includes a step of forming said second layer on the whole area of the surface of said first layer.

20. (Rejected): The method of manufacturing a hermetic sealing cap according to claim 12, wherein

said solder layer contains no Pb, and contains Ag.

(X) EVIDENCE APPENDIX

None Presented.

(XI) RELATED PROCEEDINGS APPENDIX

No related proceedings.